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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,838	09/25/2003	Daniel Alan Brokenshire	AUS920030844US1	8295

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EXAMINER	
VO, LILIAN	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,838	BROKENSHIRE ET AL.	
	Examiner	Art Unit	
	LILIAN VO	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *13 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/25/03, 11/11/05, 5/16/06, 8/15/06, 9/19/06, 10/15/06, 01/04/07, 05/20/07, 07/16/07, 10/2/07, 12/27/07, 3/30/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim 1 is pending. Claims 2 – 60 have been cancelled.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claim 1 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/670,835 in view of Washington et al. (US Pat. 5,835,775).

Although the conflicting claims are not identical, they are not patentably distinct from each other because application 10/670,835 also teaches a method for using a processor as a virtual device which comprises similar steps as being claimed in the present application.

Washington discloses creating, by the first processor, a task block in the common memory (col. 5 lines 47 – 48 "transfers the FGPS file 200 form the mass storage device 108 to the main memory 106"), the task block including a software code identifier and an input buffer address (col. 7 lines 1 – 5 "FGPS file 400 contains ..the file header 408 may contain information such as a file type identifier…a pointer to the section header table 416, the address of the FGPS file 400 to begin execution, etc"); signaling, from the first processor, the identified second processor (col. 4 lines 35 – 37 "the cpu test section 210 includes routines for determining which type of processor of a processor family is executing the FGPS file 200"), wherein the signaling includes writing the address of the task block to a mailbox corresponding to the second processor (the address of the instruction block must be written to the memory area 502 or 504 of the processors); receiving, at the second processor, the address of the task block from the second processor's mailbox (col. 8 lines 21 – 25, 29 - 40); retrieving, at the second processor, the software code identifier from the task block (col. 8 lines 29 – 40); reading data from an input buffer located in the common memory at a location corresponding to the input buffer address into the second processor's local memory (col. 8 lines 11 – 12 "allocates at least one page of main memory 106 to each processor of the computer system 100"), wherein the reading is performed using a direct memory access (DMA) operation (the operating system program is used for transferring data). Washington did not explicitly disclose the receiving a device request is at a task queue manager. Nevertheless, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify Washington's approach to include a task queue for storing request as needed to service the requests in an orderly fashion. Furthermore, it would have been obvious for one of an ordinary skill in the art at the time the invention was made to combine Washington

with application 10/670,835 to perform the method as claimed to utilize the enhance features of Washington's invention.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Washington et al. (US Pat. 5,835,775, hereinafter Washington).

6. Regarding **claim 1**, Washington discloses a computer-implemented method for managing a plurality of processors as a virtual devices, said method comprising:

receiving a device request on a first processor in a computer system, wherein the computer system includes a plurality of heterogeneous processors that share a common memory (col. 3 lines 64 – 65, col. 8 lines 16 and fig. 5) and wherein the device request corresponds to a virtual device (col. 3 lines 64 – 65, col. 5 lines 47 - 48 and col. 8 line 16);

storing data corresponding to the request in the common memory (col. 5 lines 47 - 48);

identifying a second processor from the plurality of processors to handle the request (col. 10 lines 46 – 50: "to enable task switching between different processor types, the operating system may only stop the execution…resumed on a processor of different type" – when task

switching between processors, the first processor must send request to second processor for continuing the execution of a task), wherein the first processor and the second processor are dislike processors (col. 3 lines 64-65), wherein the first processor executes a first instruction set and wherein the second processor executes a second instruction set (col. 4 lines 4 – 12);

creating, by the first processor, a task block in the common memory (col. 5 lines 47 – 48 "transfers the FGPS file 200 form the mass storage device 108 to the main memory 106"), the task block including a software code identifier and an input buffer address (col. 7 lines 1 – 5 "FGPS file 400 contains ..the file header 408 may contain information such as a file type identifier…a pointer to the section header table 416, the address of the FGPS file 400 to begin execution, etc");

signaling, from the first processor, the identified second processor (col. 4 lines 35 – 37 "the cpu test section 210 includes routines for determining which type of processor of a processor family is executing the FGPS file 200"), wherein the signaling includes writing the address of the task block to a mailbox corresponding to the second processor (the address of the instruction block must be written to the memory area 502 or 504 of the processors);

receiving, at the second processor, the address of the task block from the second processor's mailbox (col. 8 lines 21 – 25, 29 - 40);

retrieving, at the second processor, the software code identifier from the task block (col. 8 lines 29 – 40);

reading data from an input buffer located in the common memory at a location corresponding to the input buffer address into the second processor's local memory (col. 8 lines 11 – 12 "allocates at least one page of main memory 106 to each processor of the computer

system 100"), wherein the reading is performed using a direct memory access (DMA) operation (the operating system program is used for transferring data);

determining whether the software code corresponding to the software code identifier is loaded in the second processor's local memory (col. 5 lines 44 – 46); and

in response to determining that the software code corresponding to the software code identifier is not loaded in the second processor's local memory (col. 5 lines 44 – 46):

reading the software code from the common memory into the second processor's local memory (col. 5 lines 47 – 48 "transfers the FGPS file 200 from the mass storage device 108 to the main memory 106", col. 8 lines 11 - 12), wherein the reading is performed using a DMA operation (the operating system program is used for transferring data); and

processing the data by the second processor using the software code stored in the second processor's local memory (col. 5 lines 47 - 48 "schedules the process of executing the FGPS file 200 to the first processor 102").

Washington did not explicitly disclose the receiving a device request is at a task queue manager. Nevertheless, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify Washington's approach to include a task queue for storing request as needed to service the requests in an orderly fashion.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LILIAN VO whose telephone number is (571)272-3774. The examiner can normally be reached on Thursday 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

Lilian Vo
Examiner
Art Unit 2195